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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg  
Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT  
Docket No.: 303.522US1  
Filed: August 25, 1999  
Examiner: Richard A. Booth  
Serial No.: 09/382,442  
Due Date: September 20, 2001  
Group Art Unit: 2812

Commissioner for Patents  
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.  
☒ A Response Under 1.111 (2 Pages).

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 20 day of September, 2001.

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PATENT

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RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents  
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Applicant has carefully reviewed and considered the Office Action mailed on June 20, 2001, and the references cited therewith.

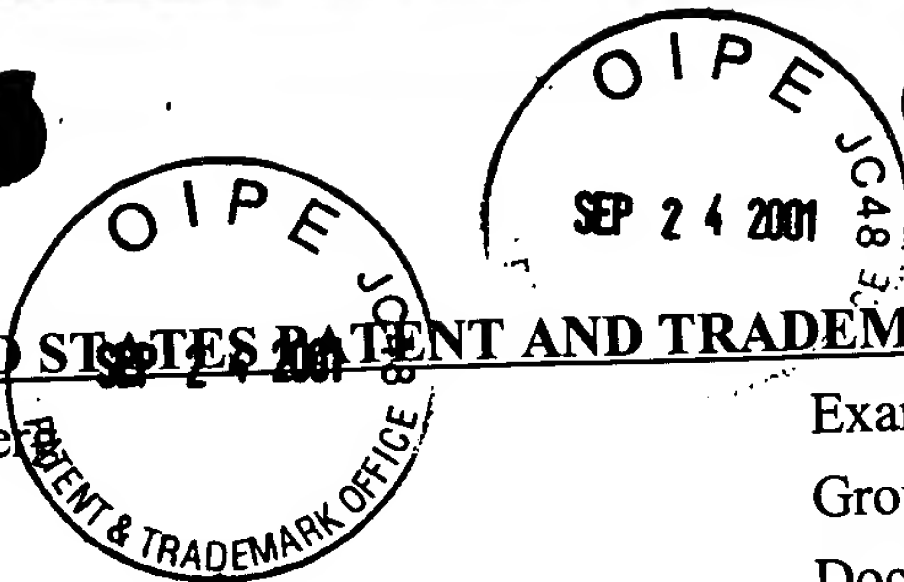
Claims 1-39 are pending in this application.

§103 Rejection of the Claims

Claims 1-14, 26-32, and 35-38 were rejected under 35 USC § 103(a) as being unpatentable over admitted prior art in view of Lisenker et al. (WO 94/19829) or Clark et al. (U.S. Patent No. 5,972,765). The Lisenker reference describes using deuterium in order to increase the bond energy of Si-H and Si-OH bonds by substituting deuterium (D). The Lisenker reference describes this procedure as usable in the fabrication of MOS transistors and bipolar junction transistors. The Clark reference describes using deuterium in the fabrication of MOSFET devices and TFT's, polyresistors and polyemitter bipolars. The Clark reference mentions that deuterium provides greater resistance to hot electron stresses.

The Examiner acknowledges that neither of the references describes a use of deuterium for reducing random single bit data loss or describes a use of deuterium in the fabrication of FLASH memory cells. The Examiner's assertion that it is obvious that a FLASH memory cell would benefit in the same way as other types of memory cells from deuterium fabrication does not account for differences in operation of a FLASH memory cell, as opposed to a MOSFET.

In a FLASH memory cell, programming operation is performed by channel hot electron injection. However, an erase operation is carried out by extracting the stored electron from the floating gate to erase gate, for all the bits, at the same time. For a FLASH memory to operate successfully, both the programming operation and the erase operation must operate in a satisfactory manner. There is no precedent in the references cited by the Examiner, to suggest



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